4463 73051

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

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Date 8/12 Serial # 09/092,174 Priority Application Date 11/20/98

Your Name M. Lewis Examiner #

AU 2899 Phone 305-3743 Room Plaza 3-3B05

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

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Other:

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What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other
Secondary Refs ___ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 11-25

Problem: See Page 1 lines 13-27
11 2 11 1-16

Solution: See structure of claims

Staff Use Only
Searcher: Derrick Reid
Searcher Phone:
Searcher Location: STIC-EIC2800, CP4-9C18
Date Searcher Picked Up: 8/16/02
Date Completed: 8/16/02
Searcher Prep/Rev Time: 2.25
Online Time: 100

Type of Search
Structure (#)
Bibliographic ✓
Litigation
Fulitext
Patent Family
Other

Vendors
STN ✓
Dialog ✓
Questel/Orbit
Lexis-Nexis
WWW/Internet
Other

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File   2:INSPEC  1969-2002/Aug W2
       (c) 2002 Institution of Electrical Engineers

Set     Items   Description
S1      22802   OPTOELECTRONIC? OR OPTO()ELECTRONIC?
S2         68   (INTERMETALLIC OR INTER()METALLIC)(2N)(SOLDER OR SOLDERING
              OR SOLDERED OR BRAZE?)
S3       2860   (GOLD OR AU) AND (TIN OR SN)
S4      19601   CI=AU EL
S5      23480   CI=SN
S6     521980   PLATINUM OR PT OR IRON OR FE OR COBALT OR CO OR NICKEL OR -
              NI
S7      17414   CI=PT
S8       4244   CI=SN EL
S9      11263   CI=PT EL
S10     26030   CI=FE EL
S11     12011   CI=CO EL
S12     20175   CI=NI EL
S13    138718   KINETIC?
S14         4   BINARY(2N) (SOLDER OR SOLDERING OR SOLDERED OR BRAZE?)
S15         6   (BINARY)(2N)(SOLDER OR SOLDERING OR SOLDERED OR BRAZ?)
S16         8   (SOLDER OR SOLDERING OR SOLDERED OR BRAZE?)(2N)(QUENCH?)
S17      1244   WET????(1N)(LAYER? OR FILM OR COAT????)
S18        83   ANTI()OXIDAT? OR ANTIOXIDAT?
S19   1083654   ENCLOS??? OR HOUS??? OR CASE? ? OR CONTAIN? OR PACK?????
S20     22697   SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
S21        42   S1 AND S3
S22         3   S1 AND (S4 AND S8)
S23        11   S21 AND (S6 OR S9:S12)
S24        10   S23 NOT S22
S25         0   S1 AND S2
S26       256   S1 AND S20
S27         2   S26 AND S13
S28         2   S27 NOT (S22 OR S23)
S29       287   S20 AND S13
S30        24   S29 AND S3
S31        24   S30 NOT (S22 OR S23 OR S27)
S32        80   S29 AND (S6 OR S9:S12)
S33        27   S32 AND EUTECTIC
S34         0   S32 AND S17
S35         0   S32 AND S18
S36         6   S32 AND TERNARY
S37        21   (S33 OR S36) NOT (S22 OR S23 OR S27 OR S30)
```

22/3,AB/1
DIALOG(R)File 2:INSPEC

6596896 INSPEC Abstract Number: A2000-12-4280K-013, B2000-06-4150-018
Title: Quasimonolithic hybridization of multiple quantum well electroabsorption modulator/detector arrays with silicon VLSI
Author(s): Callahan, J.J.; Martin, K.P.; Drabik, T.J.
Author Affiliation: Sch. of Electr. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Conference Title: 1999 IEEE LEOS Annual Meeting Conference Proceedings. LEOS'99. 12th Annual Meeting. IEEE Lasers and Electro-Optics Society 1999 Annual Meeting (Cat. No.99CH37009) Part vol.2 p.766-7 vol.2
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 2 vol. xxviii+918 pp.
ISBN: 0 7803 5634 9 Material Identity Number: XX-1999-03442
U.S. Copyright Clearance Center Code: 0 7803 5634 9/99/$10.00
Conference Title: 1999 IEEE LEOS Annual Meeting Conference Proceedings. LEOS'99. 12th Annual Meeting
Conference Date: 8-11 Nov. 1999 Conference Location: San Francisco, CA, USA
Language: English
Abstract: We report a fully inorganic technique for hybridizing MQW device arrays, that yields quasimonolithic levels of thermal conductivity, mechanical strength, and electrical parasitics, and permits a wide range of further postprocessing operations. We have demonstrated Au-Sn-based quasimonolithic hybridization to silicon VLSI of MQW electroabsorption modulators and detectors having a sophisticated vertical structure. The planarity of the process facilitates subsequent vacuum-deposition steps; the vertical device structure allows minimization of the footprint and parasitic capacitance; the chosen bond metallurgy is robust under subsequent high-temperature packaging operations. We believe that our technique offers valuable flexibility in the overall physical design of low-level optical interconnections for VLSI.
Subfile: A B

22/3,AB/2
DIALOG(R)File 2:INSPEC

5590849 INSPEC Abstract Number: B9707-0170J-034
Title: Cost effective packaging technique for multichip modules, **optoelectronic** devices, and microwave circuits
Author(s): Dohle, G.R.; Martin, K.P.; Drabik, T.J.; Callahan, J.J.
Author Affiliation: Sch. of Electr. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Conference Title: Proceedings of the 1996 International Electronics Packaging Conference p.664-70
Publisher: Int. Electron. Packaging Soc, Edina, MN, USA
Publication Date: 1996 Country of Publication: USA 681 pp.
Material Identity Number: XX96-02693
Conference Title: Proceedings of International Electronics Packaging Society Conference. 1996 Annual Conference `A Powerhouse Program'
Conference Sponsor: Int. Electron. Packaging Soc
Conference Date: 29 Sept.-1 Oct. 1996 Conference Location: Austin, TX,

USA
Language: English
Abstract: The technology of combining different semiconductor materials offers many advantages compared to single semiconductor material solutions. Epitaxial lift-off (ELO) is one of the most promising methods to address technological problems associated with combination of materials with different lattice constants. After lattice-matched growth and lift-off of a GaAs, InP or AlAs-InGaAs device, it can be subsequently transferred to another substrate. The most widely reported bonding method for ELO films is van der Waals bonding. However, there are problems with this technique, which hinder industrial use. Recently, we investigated refinements of the ELO technique using a single transparent polymer membrane to support the material during the sacrificial layer etch, then depositing Au and Sn multilayers on the lifted-off devices and new host substrate. The devices are bonded by applying heat and pressure in a reducing atmosphere. In this paper, we report our results for bonding parameter optimization, with different diffusion barriers, new multilayer structures, and new applications of the multilayer bonding technique. The bonded samples were investigated with several standard surface analysis techniques as well as mechanical tests. For further enhancement of bond quality and to reduce mechanical stress induced by thermal expansion mismatch, we investigated an annealing technique. The main advantages of our technology are given, and we show ways to further reduce costs and consider area array bonding of devices with similar coefficients of thermal expansion.
Subfile: B

22/3,AB/3
DIALOG(R)File 2:INSPEC

4468389 INSPEC Abstract Number: B9310-4270-005
Title: Reliable metallization system for flip-chip **optoelectronic** integrated circuits
Author(s): Wada, O.
Author Affiliation: Fujitsu Labs. Ltd., Atsugi, Japan
Conference Title: Materials Reliability in Microelectronics II Symposium p.155-63
Editor(s): Thompson, C.V.; LLoyd, J.R.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1992 Country of Publication: USA ix+328 pp.
Conference Date: 27 April-1 May 1992 Conference Location: San Francisco, CA, USA
Language: English
Abstract: Thermal stability of evaporated Pd, Pt and Rh films as reaction barriers to Au-Sn solder was studied for the application to flip-chip **optoelectronic** integration. Sn in the solder diffused preferentially into a barrier metal uniformly to produce more stable intermetallic phases for all three metals. Pt and Rh exhibited sufficiently small interdiffusion coefficients with high activation energies in the temperature range of device operation (Pt: 1.35 eV, Rh: 1.95 eV). This result demonstrates the usefulness of Pt and Rh in practical flip-chip integrated circuit fabrication. Aging test was conducted on flip-chip GaInAs/InP p-i-n photodiodes with Au-Sn/Pt metallization and no severe degradation was observed over 3400 h at 180 degrees C. The same metallization techniques were applied in the fabrication of 10 Gbps **optoelectronic** integrated receivers as well as quad p-i-n photodiodes for coherent optical receivers.
Subfile: B

24/3,AB/1
DIALOG(R)File 2:INSPEC

7263294 INSPEC Abstract Number: A2002-12-4280X-016, B2002-06-4190F-031
Title: Infrared transparent conductive oxides
Author(s): Johnson, L.F.; Moran, M.B.
Author Affiliation: Weapons Div., Naval Air Warfare Center, China Lake, CA, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4375 p.289-99
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2001 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2001)4375L.289:ITCO;1-C
Material Identity Number: C574-2002-003
U.S. Copyright Clearance Center Code: 0277-786X/01/$15.00
Conference Title: Window and Dome Technologies and Materials VII
Conference Sponsor: SPIE
Conference Date: 16-17 April 2001 Conference Location: Orlando, FL, USA
Language: English
Abstract: A novel class of complex metal oxides that have potential as transparent conducting oxides (TCOs) for electromagnetic-interference (EMI) shielding on IR-seeker windows and missile domes has been identified. These complex metal oxides exhibit the rhombohedral (R3m) crystalline structure of naturally occurring delafossite, CuFeO/sub 2/. The general chemical formula is ABO/sub 2/ where A is a monovalent metal (Me/sup +1/) such as Cu, Ag, **Au**, **Pt** or Pd, and B is a trivalent metal (Me/sup 3+/) such as Al, Ti, Cr, **Co**, **Fe**, **Ni**, Cs, Rh, Ga, **Sn**, In, Y, La, Pr, Nd, Sm or Eu. By adjusting the oxygen content, the conductivity can be varied over a wide range so that the delafossites behave as insulators, semiconductors or metals. This paper presents results for films of p-type Cu/sub x/Al/sub y/O/sub z/ and n-type Cu/sub x/Cr/sub y/O/sub z/ deposited by reactive magnetron **co**-sputtering from high-purity-metal targets. Films have been deposited using conventional RF- and DC-power supplies, and a new asymmetric-bipolar-pulsed-DC-power supply. Similar to the high-temperature-copper-oxide superconductors, the presence of Cu-O bonds is critical for the unique properties. Fourier transform infrared (FTIR) and electron spectroscopy for chemical analysis (ESCA) are used to understand the relationship between the **optoelectronic** properties and the molecular structure of the films. For example, FTIR absorption bands at 1470 and 1395 cm/sup -1/ are present only in Cu/sub x/Al/sub y/O/sub z/ films that exhibit enhanced electrical conductivity. When these bands are absent, the Cu/sub x/Al/sub y/O/sub z/ films have high values of resistivity. In addition to the 1470 and 1395 cm/sup -1/ bands observed in Cu/sub x/Al/sub y/O/sub z/ films, another pair of bands at 1040 and 970 cm/sup -1/ is present in Cu/sub x/Cr/sub y/O/sub z/ films.
Subfile: A B

24/3,AB/2
DIALOG(R)File 2:INSPEC

6976450 INSPEC Abstract Number: A2001-16-8115L-010, B2001-08-0520J-020

Title: **Co**-deposition of **gold-tin** alloys from a non-cyanide solution
Author(s): Doesburg, J.; Ivey, D.G.
Author Affiliation: Alberta Univ., Edmonton, Alta., Canada
Journal: Plating and Surface Finishing vol.88, no.4 p.78-83
Publisher: American Electroplaters & Surface Finishers Soc,
Publication Date: April 2001 Country of Publication: USA
CODEN: PSFMDH ISSN: 0360-3164
SICI: 0360-3164(200104)88:4L.78:DGAF;1-O
Material Identity Number: P241-2001-005
Language: English
Abstract: **Gold**-30 at.% **tin** eutectic solder is used in **optoelectronic** applications, particularly to join InP devices to submounts. The solder can be applied using solder preforms, paste, electron-beam evaporation or electrodeposition. **Co**-deposition of the solder by electroplating offers advantages over the other methods, as a simple, cost-effective technique. In this study, pulsed current electrodeposits were formed using a solution based on ammonium citrate, KAuCl/sub 4/, SnCl/sub 2/.2H/sub 2/O, sodium sulfite, L-ascorbic acid and ethylenediamine. The effects of changing the ethylenediamine and SnCl/sub 2/.2H/sub 2/O concentrations on the structure of the deposits were observed using scanning electron microscopy and X-ray diffraction. Increasing the ethylenediamine concentration in the **Au/Sn** plating solution results in increased solution stability, an increased deposition rate and a coarser grain structure. Decreasing the **Sn** content in the solution leads to a lower **Sn** content in the resulting deposit and a coarser structure. Increasing the average current density during plating affects the homogeneity of the structure in the electroplated deposit.
Subfile: A B

24/3,AB/3
DIALOG(R)File 2:INSPEC

6882906 INSPEC Abstract Number: A2001-09-8115L-022, B2001-05-0530-003
Title: Microstructural study of **co**-electroplated **Au/Sn** alloys
Author(s): Sun, W.; Ivey, D.G.
Author Affiliation: Dept. of Chem. & Mater. Eng., Alberta Univ., Edmonton, Alta., Canada
Journal: Journal of Materials Science vol.36, no.3 p.757-66
Publisher: Kluwer Academic Publishers,
Publication Date: 1 Feb. 2001 Country of Publication: USA
CODEN: JMTSAS ISSN: 0022-2461
SICI: 0022-2461(20010201)36:3L.757:MSEA;1-N
Material Identity Number: H087-2001-007
U.S. Copyright Clearance Center Code: 0022-2461/2001/$19.50
Language: English
Abstract: **Gold-tin** eutectic solder (20 wt% **Sn**), because of its excellent mechanical and thermal properties, is utilized for flip chip and laser bonding in **optoelectronic** applications. **Co**-electroplating of **Au** and **Sn** has been investigated as an alternative to conventional methods for depositing **Au/Sn** alloys. Pulse current (PC) and direct current (DC) plating tests have been performed and compared using a suitably stable plating solution. Plating conditions, including current density and ON and OFF times (for PC plating), have been varied to optimize the process. Reproducibility tests

have also been performed. It is shown that a range of alloy compositions can be deposited, including eutectic and near-eutectic compositions, with compositional and microstructural uniformity potentially suitable for microelectronic and **optoelectronic** solder applications.
Subfile: A B

24/3,AB/4
DIALOG(R)File 2:INSPEC

6741423 INSPEC Abstract Number: B2000-12-0520J-019
Title: **Co**-deposition of **Au-Sn** eutectic solder using pulsed current electroplating
Author(s): Doesburg, J.; Ivey, D.G.
Author Affiliation: Dept. of Chem. & Mater. Eng., Alberta Univ., Edmonton, Alta., Canada
Conference Title: Electrochemical Processing in ULSI Fabrication and Semiconductor/Metal Deposition II. Proceedings of the International Symposium (Electrochemical Society Proceedings Vol.99-9) p.329-39
Editor(s): Andricacos, P.C.; Searson, P.C.; Reidsema-Simpson, C.; Allongue, P.; Stickney, J.L.; Oleszek, G.M.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA ix+400 pp.
ISBN: 1 56677 231 1 Material Identity Number: XX-2000-00263
Conference Title: Proceedings of Electrochemical Processing in ULSI Fabrication and Semiconductor/Metal Deposition II
Conference Date: 3-6 May 1999 Conference Location: Seattle, WA, USA
Language: English
Abstract: **Au**-30at.**%Sn** eutectic solder is used in **optoelectronic** applications, particularly to join InP devices to the submount. The solder can be applied using solder preforms, paste, electron-beam evaporation or electrodeposition. In this study, pulsed current electrodeposits were formed using a solution based on: 200 g/l ammonium citrate, 5 g/l KAuCl/sub 4/, 2-5 g/l SnCl/sub 2/-2H/sub 2/O, 60 g/l sodium sulfite, 15 g/l L-ascorbic acid, and 0.01-0.11 M ethylene diamine. The effects of changing the ethylene diamine and SnCl/sub 2/-2H/sub 2/O concentrations on the structure of the deposits were observed using scanning electron microscopy and X-ray diffraction. The addition of ethylene diamine to the **Au/Sn** plating solution leads to a higher deposition rate, as well as a coarser grain structure. Decreasing the **Sn** content in the solution leads to a lower **Sn** content in the resulting deposit. Increasing the average current density during plating affects the homogeneity of the structure in the electroplated deposit, with a loss of preferred orientation.
Subfile: B

24/3,AB/5
DIALOG(R)File 2:INSPEC

6436190 INSPEC Abstract Number: A2000-02-8115I-021, B2000-01-0520H-021
Title: Achievement of homogeneous AuSn solder by pulsed laser-assisted deposition
Author(s): Belouet, C.; Villard, C.; Fages, C.; Keller, D.
Author Affiliation: Alcatel CIT, Marcoussis, France

Journal: Journal of Electronic Materials vol.28, no.10 p.1123-6
Publisher: TMS,
Publication Date: Oct. 1999 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(199910)28:10L.1123:AHAS;1-6
Material Identity Number: J246-1999-011
U.S. Copyright Clearance Center Code: 0361-5235/99/$7.00
Language: English
Abstract: The deposition of AuSn solder at the eutectic composition (80 wt.% **Au**, 20 wt.% **Sn**) on a wetted, chemically inert metallic barrier has been studied in relation to its use in **optoelectronic** packaging. The bonding structure, consisting of a W barrier, the top part of which is doped with **Ni** (or Ti) to provide wetting by molten AuSn, and the homogeneous 80-20 AuSn solder several micrometers thick, has been grown by the pulsed laser-assisted deposition (PLD) technique on 2" silicon wafers. The composition of the AuSn layer was controlled within better than 1 wt.% as probed by EDX across the wafer diameter. The molten solder exhibited good wetting properties on the W modified layer and the whole structure was found to be chemically stable against thermal cycling at 320 degrees C for over 3 min. The use of molten AuSn targets makes the PLD technique a most competitive one for the achievement of high quality and reliable AuSn solder.
Subfile: A B

24/3,AB/6
DIALOG(R)File 2:INSPEC

6201464 INSPEC Abstract Number: B1999-05-0170J-009
Title: First investigations of **Au/Sn** alloys on different end-metallizations
Author(s): Anhock, S.; Oppermann, H.; Kallmayer, C.; Aschenbrenner, R.; Thomas, L.; Reichl, H.
Conference Title: EuPac'98. 3rd European Conference on Electronic Packaging Technology and 9th International Conference on Interconnection Technology in Electronics p.43-6
Publisher: DVS - German Welding Soc, Dusseldorf, Germany
Publication Date: 1998 Country of Publication: Germany 196 pp.
ISBN: 3 87155 497 9 Material Identity Number: XX-1998-02748
Conference Title: Proceedings of EuPac'98. 3rd European Conference on Electronic Packaging Technology
Conference Date: 15-17 June 1998 Conference Location: Nuremberg, Germany
Language: English
Abstract: **Au-Sn** solder is becoming increasingly important in the field of microelectronic packaging. For high temperature and fluxless applications in particular, e.g. in **optoelectronics**, **Au-Sn** solder bumps are used. The **Au-Sn** solders come into contact with different end-metallization systems such as **nickel**, **platinum** or palladium used as pad-metallizations. Information about the **Au-Ni-Sn**, **Au**-Pd-**Sn** and **Au-Pt-Sn** ternary systems in terms of metallurgical fundamentals are very important for understanding and control of the technological processes. This knowledge is the base for investigations of reliability, phase formations, growth and stability, diffusion mechanisms and diffusion pathways. This paper summarizes the work done on different **Au-Ni-Sn**, **Au**-Pd-**Sn** and **Au-Pt-Sn**

alloys with maximum 20 at.% **Ni**, Pd and **Pt** contents and investigations of diffusion and interface reactions of **Au-Sn** solders on **Ni**, Pd and **Pt**. Isothermal sections of the solid state are introduced. The presence of unknown **Au-Ni-Sn** and **Au**-Pd-**Sn** phases in the tie-triangle is discussed. Results of diffusion investigations and interface reactions are shown.
Subfile: B

24/3,AB/7
DIALOG(R)File 2:INSPEC

6154879 INSPEC Abstract Number: B1999-03-0170J-035
Title: Investigations of **Au-Sn** alloys on different end-metallizations for high temperature applications [solders]
Author(s): Anhock, S.; Oppermann, H.; Kallmayer, C.; Aschenbrenner, R.; Thomas, L.; Reichl, H.
Author Affiliation: Tech. Univ. Berlin, Germany
Conference Title: Twenty Second IEEE/CPMT International Electronics Manufacturing Technology Symposium. IEMT-Europe 1998. Electronics Manufacturing and Development for Automotives (Cat. No.98CH36204) p. 156-65
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA 165 pp.
ISBN: 0 7803 4520 7 Material Identity Number: XX-1998-02802
U.S. Copyright Clearance Center Code: 0 7803 4520 7/98/$10.00
Conference Title: Twenty Second IEEE/CPMT International Electronics Manufacturing Technology Symposium. IEMT-Europe. Electronics Manufacturing and Development for Automotives
Conference Date: 27-29 April 1998 Conference Location: Berlin, Germany
Language: English
Abstract: **Au-Sn** solder is becoming increasingly important in the field of microelectronic packaging. For high temperature and fluxless applications in particular, for example in **optoelectronics**, **Au-Sn** solder bumps are used. The **Au-Sn** solders come in contact with different end-metallization systems such as **nickel**, **platinum** or palladium used as underbump-metallization. Information about the **Au-Ni-Sn**, **Au**-Pd-**Sn** and **Au-Pt-Sn** ternary systems in terms of metallurgical fundamentals are very important for understanding and controlling the technological processes. This knowledge is the base for investigations of reliability, phase formations, growth and stability, diffusion mechanisms and diffusion pathways. This paper summarizes the work done on different **Au-Ni-Sn**, **Au**-Pd-**Sn** and **Au-Pt-Sn** alloys with maximum 20 at.% **Ni**, Pd and **Pt** contents, and investigations on diffusion and interface reactions of **Au-Sn** solders on **Ni**, Pd and **Pt**. Isothermal sections of the solid state are introduced. The presence of unknown **Au-Ni-Sn** and **Au**-Pd-**Sn** phases in the tie-triangle is discussed. Results of diffusion investigations and interface reactions are shown.
Subfile: B

24/3,AB/8
DIALOG(R)File 2:INSPEC

5127431 INSPEC Abstract Number: B9601-7230C-024
Title: Design, fabrication and modeling of high-speed metal-semiconductor-metal (MSM) photodetectors with indium-**tin**-oxide (ITO) and Ti/**Pt**/**Au** contacts
Author(s): Beaulieu, C.; Gouin, F.; Noad, J.; Hartman, W.; Lisicka-Skrzek, E.; Vineberg, K.; Berolo, E.
Author Affiliation: Communication Res. Centre, Ottawa, Ont., Canada
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2397 p.534-43
Publication Date: 1995 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
U.S. Copyright Clearance Center Code: 0 8194 1744 0/95/$6.00
Conference Title: Optoelectronic Integrated Circuit Materials, Physics, and Devices
Conference Sponsor: SPIE
Conference Date: 6-9 Feb. 1995 Conference Location: San Jose, CA, USA
Language: English
Abstract: Metal-semiconductor-metal photodetectors have been fabricated on undoped epitaxial GaAs material with **gold** and indium-**tin**-oxide interdigitated contacts. In both cases, various electrode configurations were layed out with combinations of finger spacings and finger widths ranging from 1 to 3 mu m and detector cross-sections of 25*25, 50*50 and 100*100 mu m/sup 2/. Frequency response measurements were carried out up to 20 GHz. Photodetector responsivity has been plotted as a function of bias voltage. We note that for similar devices, Ti/**Pt**/**Au** contact MSMs require lower bias voltages before they reach their saturation bandwidth than ITO contact MSMs. For a 100*100 mu m/sup 2/ ITO MSM with a 2 mu m finger width and a 2 mu m finger spacing, the 3 dB bandwidth was measured to be 4 GHz at 10 V bias. By comparison, similar **gold** contact MSMs exhibit 3 dB bandwidths in excess of 12 GHz. The difference in speed is partly explained by the higher device parasitics of the ITO MSMs, as confirmed by S/sub 11/ measurements made on both types of device. The S/sub 11/ data was also used to extract the MSM equivalent circuit parameters for a high-frequency MSM model. Similar measurements on other electrode configurations show that as expected, the speed of ITO MSMs becomes considerably higher as device size is decreased, until the limit where transit-time effects start to dominate the overall performance.
Subfile: B

24/3,AB/9
DIALOG(R)File 2:INSPEC

4463764 INSPEC Abstract Number: B9309-2550F-086
Title: Reliable metallization system for flip-flop **optoelectronic** integrated circuits
Author(s): Wada, O.
Author Affiliation: Fujitsu Labs. Ltd., Atsugi, Japan
Conference Title: Advanced Metallization and Processing for Semiconductor Devices and Circuits - II. Symposium p.713-21
Editor(s): Katz, A.; Murarka, S.P.; Nissim, Y.I.; Harper, J.M.E.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1992 Country of Publication: USA xvii+965 pp.
Conference Sponsor: AT&T Bell Lab.; A.G. Associates; Air Products & Chem. ; et al

Conference Date: 27 April-1 May 1992 Conference Location: San Francisco, CA, USA
Language: English
Abstract: Thermal stability of evaporated Pd, **Pt** and Rh films as reaction barriers to **Au-Sn** solder was studied for the application to flip-chip **optoelectronic** integration. **Sn** in the solder preferentially into a barrier metal uniformly to produce more stable intermetallic phases for all three metals. **Pt** and Rh exhibited sufficiently small interdiffusion coefficients with high activation energies in the temperature range of device operation (**Pt**: 1.35 eV, Rh: 1.95 eV). This result demonstrates the usefulness of **Pt** and Rh in practical flip-chip integrated circuit fabrication. An aging test was conducted on flip-chip GaInAs/InP p-i-n photodiodes with **Au-Sn/ Pt** metallization and no severe degradation was observed over 3400 h at 180 degrees C. The same metallization techniques were applied in the fabrication of 10 Gbps **optoelectronic** integrated receivers as well as quad p-i-n photodiodes for coherent optical receivers.
Subfile: B

24/3,AB/10
DIALOG(R)File 2:INSPEC

02628462 INSPEC Abstract Number: B86023844
Title: High-speed optical repeater ICs
Author(s): Kamoto, T.; Kanamori, S.; Kawarada, K.; Nagano, J.
Author Affiliation: NTT, Tokyo, Japan
Journal: Electrical Communication Laboratories Technical Journal vol.34, no.10 p.1453-62
Publication Date: 1985 Country of Publication: Japan
CODEN: TJECAS ISSN: 0415-3200
Language: Japanese
Abstract: Repeater circuits for a high-speed optical transmission system are integrated on six monolithic chips using Si shallow junction bipolar devices with 5-6 GHz f/sub T/. To achieve the high reliability essential for submarine use, a two-level metallization structure is introduced which utilizes Cu-doped Al and **Au/Pt**/Ti in conjunction with a **TiN** diffusion barrier. Sufficient performance measurements are achieved. The transimpedance and bandwidth of the equalizing amplifier IC are 91 dB and 310 MHz, respectively. The timing amplifier IC phase deviation is kept within 10 degrees. The decision IC sensitivity is less than 3%. Overall field experiments confirm that an efficient 400 Mb/s optical repeater system can be constructed using these IC's.

28/3,AB/1
DIALOG(R)File 2:INSPEC

6786364 INSPEC Abstract Number: B2001-01-0100-044
Title: Two Symposia - Packaging and **Soldering** Technologies for Electronic Interconnects and Materials Issues in Microelectronics: Optical, Electrical and Thermal
Journal: Journal of Electronic Materials vol.29, no.10
Publisher: TMS; IEEE,
Publication Date: Oct. 2000 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
Material Identity Number: J246-2000-010
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Conference Title: Two Symposia - Packaging and Soldering Technologies for Electronic Interconnects and Materials Issues in Microelectronics: Optical, Electrical and Thermal
Conference Sponsor: TMS - Miner. Metals & Mater. Soc
Conference Date: 12-16 March 2000 Conference Location: Nashville, TN, USA
Language: English
Abstract: The intent of the **soldering** and packaging symposium was to examine the rapid advances in the following areas relevant to interconnections in microelectronics: (a) packaging and **soldering** technologies, (b) applications of multicomponent phase equilibria in electronic packaging, (c) **kinetics** of interfacial reaction in **solder** joints, (d) interfacial reaction and reliability of **solder** joints, and (e) reliability of bulk solders. Some of the key intents of the materials in microelectronics symposium were to examine the state-of-the-art knowledge in the following areas: (a) alpha particle issues in microelectronic packaging and materials, (b) low alpha Pb and applications, and (c) the impact of other materials on microelectronic and **optoelectronic** packaging.
Subfile: B

28/3,AB/2
DIALOG(R)File 2:INSPEC

5894531 INSPEC Abstract Number: B9805-0170J-060
Title: The influence of microstructure on the failure of eutectic solders
Author(s): Morris, J.W., Jr.; Reynolds, H.L.
Author Affiliation: Dept. of Mater. Sci., California Univ., Berkeley, CA, USA
Conference Title: Design and Reliability of Solders and Solder Interconnections. Proceedings of a Symposium held during the TMS Annual Meeting p.49-58
Editor(s): Mahidhara, R.K.; Frear, D.R.; Sastry, S.M.L.; Murty, K.L.; Liaw, P.K.; Winterbottom, W.L.
Publisher: TMS, Warrendale, PA, USA
Publication Date: 1997 Country of Publication: USA xi+448 pp.
ISBN: 0 87339 354 6 Material Identity Number: XX98-00492
Conference Title: Design and Reliability of Solders and Solder Interconnections. Proceedings of a Symposium held during the TMS Annual Meeting
Conference Sponsor: TMS

Conference Date: 10-13 Feb. 1997 Conference Location: Orlando, FL, USA
Language: English

Abstract: There are three key failure mechanisms during the life of microelectronic **solder** joints: overload failure during handling, thermal fatigue failure during service, and, particularly in the case of joints for **optoelectronic** devices, dimensional changes during service. Each of these failure modes is strongly influenced by the **solder** microstructure, which is, in turn, affected by the **solder** composition, the chemical nature of the substrate, and the manufacturing process that is used to create the **solder** joint. This paper discusses the varieties of microstructures that are found in common **solder** joints, their influence on lifetime and failure mode, and the metallurgical techniques that can be used to control microstructure and modify the nature and **kinetics** of **solder** joint failure.

37/3,AB/1
DIALOG(R)File 2:INSPEC

7254527 INSPEC Abstract Number: B2002-06-0530-003
Title: Intermetallic compounds formed during the **soldering** reactions of **eutectic** Sn-9Zn with Cu and **Ni** substrates
Author(s): Chan, Y.C.; Chiu, M.Y.; Chuang, T.H.
Author Affiliation: Dept. of Mater. Sci. & Eng., Nat. Taiwan Univ., Taipei, Taiwan
Journal: Zeitschrift fur Metallkunde vol.93, no.2 p.95-8
Publisher: Carl Hanser GmbH,
Publication Date: Feb. 2002 Country of Publication: Germany
CODEN: ZEMTAE ISSN: 0044-3093
SICI: 0044-3093(200202)93:2L.95:ICFD;1-#
Material Identity Number: Z021-2002-003
Language: English
Abstract: This study investigates the morphology and growth **kinetics** of the intermetallic compounds formed during the interfacial reactions of **eutectic** Sn-9Zn solders with Cu and **Ni** substrates at temperatures ranging from 250 to 350 degrees C. Experimental results show that the intermetallic growth rate at the Sn-9Zn/Cu interface is much higher than that at the Sn-9Zn/**Ni** interface. **Kinetics** analyses indicate that both types of interfacial reactions are diffusion-controlled. The activation energies for the intermetallic growth at the Sn-9Zn/Cu and Sn-9Zn/**Ni** interfaces are 8.2 and 68.9 kJ/mol, respectively. The formation mechanisms of the intermetallic compounds during the **soldering** reactions at both interfaces are clarified by using a Ta thin film as diffusion marker.
Subfile: B

37/3,AB/2
DIALOG(R)File 2:INSPEC

7133874 INSPEC Abstract Number: B2002-02-0170J-012
Title: Microstructure coarsening during static annealing of 60Sn40Pb **solder** joints. II. **Eutectic** coarsening **kinetics**
Author(s): Kang Jung; Conrad, H.
Author Affiliation: Dept. of Mater. Sci. & Eng., North Carolina State Univ., Raleigh, NC, USA
Journal: Journal of Electronic Materials vol.30, no.10 p.1303-7
Publisher: TMS; IEEE,
Publication Date: Oct. 2001 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(200110)30:10L.1303:MCDS;1-Q
Material Identity Number: J246-2001-012
U.S. Copyright Clearance Center Code: 0361-5235/01/$7.00
Language: English
Abstract: For **pt** . I see ibid., vol. 30, no. 10, p. 1294-1302 (2001). The **eutectic** coarsening **kinetics** for 60Sn40Pb **solder** joints annealed at 50 degrees C to 150 degrees C was determined to be of the form D/sup n/-D/sup n//sub 0/=K/sub 0/ exp(-Q/RT)t where D is the mean linear intercept phase size, D/sub 0/ approximately=1.0 mu m the as-reflowed phase size, n=4.1+or-0.15, Q=39.8+or-0.8 kJ/mole,

K/sub 0/=1*10/sup -23/-4.5*10/sup -23/ m/sup 4//s, and t the time. The magnitude of the phase size exponent, n, and the parameters, K/sub 0/ and Q, are in accord with the models by Senkov and Myshlyaev and by Ardell for phase coarsening controlled by grain boundary or interfacial solute diffusion. The phase shape factor did not have a significant influence on the coarsening **kinetics**.
Subfile: B

37/3,AB/3
DIALOG(R)File 2:INSPEC

6835533 INSPEC Abstract Number: B2001-03-0170G-004
Title: Coarsening **kinetics** of **Ni**/sub 3/Sn/sub 4/ scallops during interfacial reaction between liquid **eutectic** solders and Cu/**Ni**/Pd metallization
Author(s): Ghosh, G.
Author Affiliation: Dept. of Mater. Sci. & Eng., Northwestern Univ., Evanston, IL, USA
Journal: Journal of Applied Physics vol.88, no.11 p.6887-96
Publisher: AIP,
Publication Date: 1 Dec. 2000 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(20001201)88:11L.6887:CKNS;1-1
Material Identity Number: J004-2000-022
U.S. Copyright Clearance Center Code: 0021-8979/2000/88(11)/6887(10)/$17.00
Language: English
Abstract: The thickening and radial growth **kinetics** of **Ni**/sub 3/Sn/sub 4/ scallops formed during interfacial reaction between liquid **eutectic** solders and electroplated **Ni**/Pd metallization scheme on Cu substrate is studied. Selective etching of **solder** revealed three-dimensional morphology, and the dynamical phenomena, such as faceting, competitive growth, and coalescence of **Ni**/sub 3/Sn/sub 4/ scallops during interfacial reaction. The growth **kinetics** of the **Ni** /sub 3/Sn/sub 4/ scallops in the submicron length scale was analyzed using an Arrhenius-type of equation. Both **kinetics** exhibited nonparabolic behavior with the time exponent greater than three. The thickening of the **Ni** /sub 3/Sn/sub 4/ layer during interfacial reaction was accompanied by the concomitant coarsening of the scallops. The coarsening **kinetics** during early stages of interfacial reaction was characterized by (i) a temporal law with the time exponent greater than three, (ii) a decrease in the average number of scallops per unit volume with reaction time, and (iii) an increase in the standard deviation of the normalized size distribution with reaction time. The temporal laws for growth **kinetics** are discussed in terms of the effects of characteristic microstructural length scale and the existing coarsening theories. Among the coarsening theories, both the temporal law and the characteristics of radial size distributions were found to be consistent with the predictions of a recent Monte Carlo simulation of liquid-phase sintering in a two-phase system where the volume fraction of the second phase was very high.
Subfile: B

37/3,AB/4

DIALOG(R)File 2:INSPEC

6815706 INSPEC Abstract Number: A2001-04-6822-008
Title: Formation and growth of interfacial intermetallic layers in **eutectic** Sn-Ag **solder** and its composite **solder** joints
Author(s): Choi, S.; Lucas, J.P.; Subramanian, K.N.; Bieler, T.R.
Author Affiliation: Dept. of Mater. Sci. & Mech., Michigan State Univ., East Lansing, MI, USA
Journal: Journal of Materials Science: Materials in Electronics vol.11, no.6 p.497-502
Publisher: Kluwer Academic Publishers/Chapman & Hall,
Publication Date: Aug. 2000 Country of Publication: USA
CODEN: JSMEEV ISSN: 0957-4522
SICI: 0957-4522(200008)11:6L.497:FGII;1-X
Material Identity Number: H206-2001-001
U.S. Copyright Clearance Center Code: 0957-4522/2000/$15.00
Language: English
Abstract: Single shear lap joints were made by **soldering** two Cu substrates with **eutectic** Sn-Ag **solder** , and its composite solders containing FeSn/FeSn/sub 2/ or **Ni** /sub 3/Sn/sub 2/ intermetallic particles introduced by an in-situ method. Ageing of **solder** joints was performed at 70, 100, 120, 150, 180 degrees C for 1400 h. The growth of the interfacial intermetallic compound (IMC) layers was characterized assuming diffusion-controlled growth **kinetics**. Effects of such FeSn/FeSn/sub 2/ and **Ni**/sub 3/Sn/sub 4/ particulates on the IMC layer growth rate were extensively characterized. Composite **solder** joints in the fabricated condition formed thinner IMC layers compared to the corresponding non-composite **solder** joints. The Cu/sub 6/Sn/sub 5/ IMC layer grew faster at temperatures above 120 degrees C (T/T/sub m/=0.8), while growing slower at temperatures below 120 degrees C in composite **solder** joints. In-situ introduced FeSn/FeSn/sub 2/ and **Ni**/sub 3/Sn/sub 4/ particle reinforcements in composite **solder** joints proved effective in reducing the overall growth of the interfacial Cu/sub 6/Sn/sub 5/ IMC layer only at lower temperatures. Composite **solder** joints exhibited slower growth of the Cu/sub 3/Sn layer during ageing at all temperatures used in this study. Two different regions having different activation energies depending on the temperature were identified for the growth of Cu/sub 6/Sn/sub 5/ and Cu/sub 3/Sn IMC layers.
Subfile: A

37/3,AB/5
DIALOG(R)File 2:INSPEC

6781263 INSPEC Abstract Number: A2001-02-6822-010, B2001-01-0530-005
Title: Long-term aging study on the solid-state reaction between 58Bi42Sn **solder** and **Ni** substrate
Author(s): Chen, C.; Ho, C.E.; Lin, A.H.; Luo, G.L.; Kao, C.R.
Author Affiliation: Dept. of Chem. Eng., Nat. Central Univ., Chung-Li, Taiwan
Journal: Journal of Electronic Materials Conference Title: J. Electron. Mater. (USA) vol.29, no.10 p.1200-6
Publisher: TMS; IEEE,
Publication Date: Oct. 2000 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(200010)29:10L.1200:LTAS;1-U

Material Identity Number: J246-2000-010
U.S. Copyright Clearance Center Code: 0361-5235/2000/$7.00
Conference Title: Two Symposia - Packaging and Soldering Technologies for Electronic Interconnects and Materials Issues in Microelectronics: Optical, Electrical and Thermal
Conference Sponsor: TMS - Miner. Metals & Mater. Soc
Conference Date: 12-16 March 2000 Conference Location: Nashville, TN, USA
Language: English
Abstract: The reaction between **Ni** and **eutectic** BiSn **solder** at 85 degrees C, 100 degrees C, 120 degrees C, and 135 degrees C was studied. Reaction times ranging from 25 h to 3600 h were used. Only **Ni** /sub 3/Sn/sub 4/ was detected as a result of the reaction. None of the other **Ni**-Sn intermetallic compounds and none of the **Ni**-Bi intermetallic compounds were observed. The growth of **Ni**/sub 3/Sn/sub 4/ followed diffusion-controlled **kinetics** and was very slow, with the layer thickness reaching only 16 mu m after 3600 h of aging at 135 degrees C. The **eutectic** BiSn microstructure coarsened very quickly. Substantial coarsening can be observed at 135 degrees C for only 200 h of aging. In addition, fine Bi-rich particles within the Sn-rich phase of the **solder** were found. The amount of these fine Bi-rich particles increased with the aging temperature. It is believed that the formation of these fine Bi-rich particles is due to the fact that the Sn-rich phase can dissolve substantial amounts of Bi. It was also found that, as aging time increased, the region immediately adjacent to the **Ni**/sub 3/Sn/sub 4/ layer was preferentially occupied by the Bi-rich phase. This is because Sn in that region had reacted with **Ni** to form **Ni**/sub 3/Sn/sub 4/, leaving a nearly continuous Bi-rich phase above the **Ni**/sub 3/Sn/sub 4/. Since Bi-rich alloys tend to be brittle, a nearly continuous Bi-rich phase might weaken the strength of a **solder** joint. The **Ni**/sub 3/Sn/sub 4/ grain size increased gradually from the **Ni**/**Ni**/sub 3/Sn/sub 4/ interface to the **Ni**/sub 3/Sn/sub 4//BiSn interface, which is probably an Ostwald ripening phenomenon.
Subfile: A B

37/3,AB/6
DIALOG(R)File 2:INSPEC

6781261 INSPEC Abstract Number: A2001-02-8190-005, B2001-01-0170G-011
Title: A comparative study of the **kinetics** of interfacial reaction between **eutectic** solders and Cu/**Ni**/Pd metallization
Author(s): Ghosh, G.
Author Affiliation: Dept. of Mater. Sci. & Eng., Northwestern Univ., Evanston, IL, USA
Journal: Journal of Electronic Materials Conference Title: J. Electron. Mater. (USA) vol.29, no.10 p.1182-93
Publisher: TMS; IEEE,
Publication Date: Oct. 2000 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(200010)29:10L.1182:CSKI;1-R
Material Identity Number: J246-2000-010
U.S. Copyright Clearance Center Code: 0361-5235/2000/$7.00
Conference Title: Two Symposia - Packaging and Soldering Technologies for Electronic Interconnects and Materials Issues in Microelectronics: Optical, Electrical and Thermal
Conference Sponsor: TMS - Miner. Metals & Mater. Soc

Conference Date: 12-16 March 2000 Conference Location: Nashville, TN, USA
Language: English
Abstract: A comparative study of the **kinetics** of interfacial reaction between the **eutectic** solders (Sn-3.5Ag, Sn-57Bi, and Sn-38Pb) and electroplated **Ni**/Pd on Cu substrate (Cu/**Ni**/NiPd/**Ni** /Pd) was performed. The interfacial microstructure was characterized by imaging and energy dispersive x-ray analysis in scanning electron microscope (SEM). For a Pd-layer thickness of less than 75 nm, the presence or the absence of Pd-bearing intermetallic was found to be dependent on the reaction temperature. In the case of Sn-3.5Ag **solder** , we did not observe any Pd-bearing intermetallic after reaction even at 230 degrees C. In the case of Sn-57Bi **solder** the PdSn/sub 4/ intermetallic was observed after reaction at 150 degrees C and 180 degrees C, while in the case of Sn-38Pb **solder** the PdSn/sub 4/ intermetallic was observed after reaction only at 200 degrees C. The PdSn/sub 4/ grains were always dispersed in the bulk **solder** within about 10 mu m from the **solder** /substrate interface. At higher reaction temperatures, there was no Pd-bearing intermetallic due to increased solubility in the liquid **solder** . The presence or absence of Pd-bearing intermetallic was correlated with the diffusion path in the calculated Pd-Sn-X (X=Ag, Bi, Pb) isothermal sections. In the presence of unconsumed **Ni**, only **Ni**/sub 3/Sn/sub 4/ intermetallic was observed at the **solder** -substrate interface by SEM. The presence of **Ni**/sub 3/Sn/sub 4/ intermetallic was consistent with the expected diffusion path based on the calculated **Ni** -Sn-X (X=Ag, Bi, Pb) isothermal sections. Selective etching of solders revealed that **Ni**/sub 3/Sn/sub 4/ had a faceted scallop morphology. Both the radial growth and the thickening **kinetics** of **Ni**/sub 3/Sn/sub 4/ intermetallic were studied. In the thickness regime of 0.14 mu m to 1.2 mu m, the growth **kinetics** always yielded a time exponent n>3 for liquid-state reaction. The temporal law for coarsening also yielded time exponent m>3. The apparent activation energies for thickening were: 16936 J/mol for the Sn-3.5Ag **solder**, 17804 J/mol for the Sn-57Bi **solder**, and 25749 J/mol for the Sn-38Pb **solder** during liquid-state reaction. The corresponding activation energies for coarsening were very similar. However, an apparent activation energy of 37599 J/mol was obtained for the growth of **Ni**/sub 3/Sn/sub 4/ intermetallic layer during solid-state aging of the Sn-57Bi/substrate diffusion couples. The **kinetic** parameters associated with thickening and radial growth were discussed in terms of current theories.
Subfile: A B

37/3,AB/7
DIALOG(R)File 2:INSPEC

6724366 INSPEC Abstract Number: A2000-22-6822-001, B2000-11-2550F-068
Title: Interfacial microstructure and the **kinetics** of interfacial reaction in diffusion couples between Sn-Pb **solder** and Cu/**Ni**/Pd metallization
Author(s): Ghosh, G.
Author Affiliation: Dept. of Mater. Sci. & Eng., Northwestern Univ., Evanston, IL, USA
Journal: Acta Materialia vol.48, no.14 p.3719-38
Publisher: Elsevier,
Publication Date: 4 Sept. 2000 Country of Publication: UK
CODEN: AMATEB ISSN: 1359-6454

SICI: 1359-6454(20000904)48:14L.3719:IMKI;1-3
Material Identity Number: G397-2000-015
U.S. Copyright Clearance Center Code: 1359-6454/2000/$20.00
Language: English
Abstract: The interfacial microstructure and the **kinetics** of interfacial reaction between **eutectic** Sn-Pb **solder** and electroplated **Ni**/Pd on a Cu substrate have been studied by scanning, transmission and analytical electron microscopies. Besides PdSn/sub 4/ and **Ni**/sub 3/Sn/sub 4/, small grains of **Ni**/sub 3/Sn/sub 2/ with a hexagonal structure are also observed after long-time aging of the diffusion couples at 125 degrees C. The presence of intermetallic phases is correlated with the diffusion paths in the calculated Pd-Pb-Sn and **Ni** -Pb-Sn isothermal sections. The growth **kinetics** of the **Ni**/sub 3/Sn/sub 4/ scallops in the submicrometer length scale was analyzed with an Arrhenius type of equation. The thickening **kinetics** yields a time exponent n=3.1 and an apparent activation energy (Q/sub h/) of 25750 J/mol, while the radial growth **kinetics** data yield a time exponent m approximately=6.6 and an apparent activation energy (Q/sub d/) of 15300 J/mol. The radial size distributions (RSDs) of **Ni**/sub 3/Sn/sub 4/ scallops were also quantified. The parameters describing RSDs are consistent with the theories of coarsening in two-phase systems containing a very high volume fraction of the second phase. Selective etching of **solder** revealed the three-dimensional morphology of PdSn/sub 4/ and **Ni** /sub 3/Sn/sub 4/, and also the dynamical phenomena, such as faceting, competitive growth and coalescence of **Ni**/sub 3/Sn/sub 4/ scallops during interfacial reaction. Non-parabolic growth **kinetics** are discussed in terms of the existing theories and characteristics of the evolving microstructure.
Subfile: A B

37/3,AB/8
DIALOG(R)File 2:INSPEC

6721859 INSPEC Abstract Number: B2000-11-2210D-017
Title: Intermetallic phase formation and growth **kinetics** at the interface between molten **solder** and **Ni**-containing under bump metallization
Author(s): Su, P.; Korhonen, T.; Korhonen, M.; Li, C.-Y.
Author Affiliation: Dept. of Mater. Sci. & Eng., Cornell Univ., Ithaca, NY, USA
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.1712-18
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: Direct Chip Attach (DCA) of Si chips to an organic substrate requires modification to the conventional Cu based Under Bump Metallization (UBM). **Ni** -containing UBM's have proven to be able to effectively

reduce the intermetallic compound growth rate, which in turn reduces the consumption of the wetting metals in the UBM during the reaction between the **solder** and the UBM. In this research, the microstructure evolution of the interface between molten **eutectic** Pb/Sn **solder** and several alloy-foils with different Cu/**Ni** ratios is studied. The experimental results show that the low diffusivity and dissolution rate of **Ni** play important roles in restricting the growth of the intermetallic and changing the interface morphology. A **kinetic** model is proposed for the Intermetallic Compound (IMC) growth based on the Cu-**Ni**/**solder** reaction, and is applied to analyze the data from UBM/**solder** experiments.
Subfile: B

37/3,AB/9
DIALOG(R)File 2:INSPEC

6551451 INSPEC Abstract Number: B2000-05-0170J-027
Title: Fine pitch low-cost bumping for flip chip technology
Author(s): Szu-Wei Lu; Ruoh-Huey Uang; Kuo-Chuan Chen; Hsu-Tien Hu; Ling-Chen Kung; Hsin-Chien Huang
Author Affiliation: Dept. for Packaging Process, Ind. Technol. Res. Inst., Hsinchu, Taiwan
Conference Title: Twenty Fourth IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No.99CH36330) p.127-30
Publisher: IEEE, Piscataway, NJ,USA
Publication Date: 1999 Country of Publication: USA xiv+479 pp.
ISBN: 0 7803 5502 4 Material Identity Number: XX-1999-02924
U.S. Copyright Clearance Center Code: 0 7803 5502 4/99/$10.00
Conference Title: Twenty Fourth IEEE/CPMT International Electronics Manufacturing Technology Symposium
Conference Sponsor: IEEE; Semicond. Equipment and Mater. Int
Conference Date: 18-19 Oct. 1999 Conference Location: Austin, TX, USA
Language: English
Abstract: In this paper, a low-cost and fine pitch bumping process by electroless **Ni** -Au bumping for the UBM (under bump metallurgy) and stencil printing for the **solder** bump is studied. The **solder** bumps are made of **eutectic** SnPb. The pitches of the **solder** bumps range from 300 mu m to 200 mu m for various stencil openings from 210 mu m to 125 mu m. The regular bump height is 90 mu m for the 200 mu m pitch. The pad opening size is also controlled as a variable. The **kinetics** of zincating on an Si-Cu surface and on an Al surface are compared. It is found that zincating replacement on the Al-Si-Cu surface is much more rapid than on the Al surface and the dissolution rate of Al-Si-Cu is also faster than that of Al. Finally, the quality of the low-cost **solder** bumping process is evaluated by shear tests and reliability tests.
Subfile: B

37/3,AB/10
DIALOG(R)File 2:INSPEC

6480055 INSPEC Abstract Number: B2000-03-0170J-005
Title: **Kinetics** of interfacial reaction between **eutectic** Sn-Pb

solder and Cu/**Ni**/Pd metallizations
Author(s): Ghosh, G.
Author Affiliation: Dept. of Mater. Sci. & Eng., Northwestern Univ., Evanston, IL, USA
Journal: Journal of Electronic Materials Conference Title: J. Electron. Mater. (USA) vol.28, no.11 p.1238-50
Publisher: TMS,
Publication Date: Nov. 1999 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(199911)28:11L.1238:KIRB;1-R
Material Identity Number: J246-1999-012
U.S. Copyright Clearance Center Code: 0361-5235/99/$7.00
Conference Title: InterconnectPACK. Interconnections for Electronic Packaging
Conference Sponsor: TMS - Miner. Metals & Mater. Soc
Conference Date: 28 Feb.-4 March 1999 Conference Location: San Diego, CA, USA
Language: English
Abstract: The interfacial microstructure and reaction **kinetics** between **eutectic** Sn-Pb **solder** and electroplated **Ni**/Pd on a Cu substrate (Cu/**Ni**/NiPd/**Ni** /Pd) were studied in both the liquid and solid **solder** states. The liquid-state reaction was carried out at 200 degrees C, 225 degrees C, and 250 degrees C for 30 s, 60 s, 150 s, and 300 s at each temperature. Solid-state aging was carried out at 125 degrees C for up to 43 days. The interfacial microstructure was characterized by imaging and EDX analysis in the SEM. Depending on the Pd layer thickness, both PdSn/sub 4/ and PdSn/sub 3/ phases were observed near the **solder** -substrate interface. These results were correlated with the initial Pd layer thickness and the diffusion path in the calculated Pd-Pb-Sn isothermal sections. For these isothermal reactions, only one **Ni**-bearing intermetallic (**Ni**/sub 3/Sn/sub 4/) was observed at the **solder**-substrate interface. The presence of **Ni**/sub 3/Sn/sub 4/ was consistent with the expected diffusion path based on the calculated **Ni**-Pb-Sn isothermal sections. Selective **solder** etching revealed that PdSn/sub 4/ and PdSn/sub 3/ had a faceted rod morphology, and **Ni** /sub 3/Sn/sub 4/ had a faceted scallop morphology which gave rise to a rugged **Ni**/sub 3/Sn/sub 4/-**solder** interface. Pb segregation on the facets of PdSn/sub 4/ and PdSn/sub 3/ was also observed. The **Ni** /sub 3/Sn/sub 4/ layer growth **kinetics** at the **solder**-substrate interface were analyzed via an Arrhenius-type equation. In the 0.16-1.2 mu m thickness range, the growth **kinetics** yielded a time exponent n=3.1, an apparent activation energy of 9260 J/mol in both liquid and solid states, and a temperature dependent pre-exponential factor. The latter was attributed to the presence of one or more phases ahead of the growing layer.
Subfile: B

37/3,AB/11
DIALOG(R)File 2:INSPEC

6317033 INSPEC Abstract Number: A1999-18-6822-002
Title: **Kinetic** analysis of interfacial diffusion accompanied by intermetallic compound formation
Author(s): Kim, P.G.; Jang, J.W.; Tu, K.N.; Frear, D.R.
Author Affiliation: Dept. of Mater. Sci. & Eng., California Univ., Los Angeles, CA, USA

Journal: Journal of Applied Physics vol.86, no.3 p.1266-72
Publisher: AIP,
Publication Date: 1 Aug. 1999 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19990801)86:3L.1266:KAID;1-U
Material Identity Number: J004-1999-014
U.S. Copyright Clearance Center Code: 0021-8979/99/86(3)/1266(7)/$15.00
Language: English
Abstract: In interfacial reactions, a short-circuit diffusion along grain boundaries or interfaces can be accompanied by intermetallic compound formation. The compound penetrates the grain boundaries or the interfaces. This is a generic reliability issue for layered thin film structures because it causes a decrease in adhesion strength of the thin films. We have modified Fisher's grain boundary diffusion model to include this reactive **kinetic** process, and an analytical solution was obtained. A t/sup 1/4/ dependence of penetration is found, the same as Fisher's model. The important **kinetic** parameters in the solutions are a diffusion coefficient along the short-circuit path, an intrinsic interdiffusion coefficient in the compound, and a partition coefficient. A comparison between the calculated and measured data from the lateral penetration of **eutectic** SnPb **solder** along the interface between electroless **Ni** and oxysilicon nitride dielectric, accompanied by **Ni**/sub 3/Sn/sub 4/ compound formation, is given.
Subfile: A

37/3,AB/12
DIALOG(R)File 2:INSPEC

6291598 INSPEC Abstract Number: A1999-16-8190-001
Title: Thermal stability and **brazing** characteristics of Zr/sub 0.7-x/M/sub x/Be/sub 0.3/ (M=Ti or Nb) **ternary** amorphous filler metals
Author(s): Han, Y.-S.; Park, C.-H.; Jang, K.-J.; Bae, C.-H.; Choi, C.-B.; Lee, J.-Y.
Author Affiliation: Dept. of Mater. Sci. & Eng., Korea Adv. Inst. of Sci. & Technol., Taejon, South Korea
Journal: Journal of Nuclear Materials vol.270, no.3 p.334-41
Publisher: Elsevier,
Publication Date: April 1999 Country of Publication: Netherlands
CODEN: JNUMAM ISSN: 0022-3115
SICI: 0022-3115(199904)270:3L.334:TSBC;1-W
Material Identity Number: J093-1999-009
U.S. Copyright Clearance Center Code: 0022-3115/99/$20.00
Language: English
Abstract: The effects of Ti or Nb substitution on the thermal stability and **brazing** characteristics of Zr/sub 0.7-x/M/sub x/Be/sub 0.3/ (M=Ti or Nb) **ternary** amorphous alloys were investigated in order to improve properties of Zr-Be binary amorphous alloy as a new filler metal for joining zirconium alloy. The Zr/sub 0.7-x/M/sub x/Be/sub 0.3/ (M=Ti or Nb, 0<or=x<or=0.1) **ternary** amorphous alloys were produced by melt-spinning method. In the selected compositional range, the thermal stability of Zr/sub 0.7-x/Ti/sub x/Be/sub 0.3/ and Zr/sub 0.7-x/Nb/sub x/Be/sub 0.3/ amorphous alloys are improved by the substitution of titanium or niobium for zirconium. As the Ti and Nb content increases, the crystallization temperatures increase from 610 degrees C to 717 degrees C and 610 degrees C to 678 degrees C, respectively. These amorphous alloys

were put into practical use in joining bearing pads on zircaloy cladding sheath. Using Zr-Ti-Be amorphous alloys as filler metals, smooth interface and spherical primary particles (proeutectic phase) appear in the **brazed** layer, which is the similar microstructure of using Zr/sub 0.7/Be/sub 0.3/ binary amorphous alloys. In the case of Zr-Nb-Be amorphous alloys, **Ni** -precipitated Zr phase that may cause some degradation in ductility and corrosion-resistance is formed at both sides of the **brazed** layer.
Subfile: A

37/3,AB/13
DIALOG(R)File 2:INSPEC

6073768 INSPEC Abstract Number: A9824-6822-006
Title: Growth **kinetic** studies of Cu-Sn intermetallic compound and its effect on shear strength of LCCC SMT **solder** joints
Author(s): Chan, Y.C.; So, A.C.K.; Lai, J.K.L.
Author Affiliation: Dept. of Electron. Eng., City Univ., Kowloon, Hong Kong
Journal: Materials Science & Engineering B (Solid-State Materials for Advanced Technology) vol.B55, no.1-2 p.5-13
Publisher: Elsevier,
Publication Date: 14 Aug. 1998 Country of Publication: Switzerland
CODEN: MSBTEK ISSN: 0921-5107
SICI: 0921-5107(19980814)B55:1/2L.5:GKSI;1-1
Material Identity Number: M712-98010
U.S. Copyright Clearance Center Code: 0921-5107/98/$19.00
Language: English
Abstract: Growth **kinetics** of interfacial Cu-Sn intermetallic (IMC) layer and its effect on the shear strength on practical LCCC surface mount **solder** joints were studied for isothermal aging at 70, 120, 155 and 170 degrees C. Only normal Cu/sub 6/Sn/sub 5/(eta -phase) intermetallic was found in the interfacial IMC layer of as-**soldered solder** joint, whereas the duplex structure of both eta -phase and epsilon -phase Cu/sub 3/Sn existed in all annealed joints. The growth **kinetics** of the overall interfacial IMC layer can simply be described by classical **kinetic** theory for solid-state diffusional growth with an activation energy of 1.09 eV and interdiffusion coefficient of 1.6110/sup -4/ m/sup 2/ s/sup -1/. The relatively higher activation energy, as compared with that found for bi-metallic couple of **eutectic** Sn-Pb **solder** on copper, is attributed to the dissolution of **Ni** from the component metallization into the bulk Sn-Pb **solder**. In addition, the shear fractures in all the **solder** joints investigated are shown to be ductile in nature and confined in the bulk **solder** rather than through the interfacial IMC layer. A linear reduction in shear joint strength was observed with an increase in intermetallic layer thickness up to ~5.6 mu m. Such a reduction in joint strength is due to a continuous removal of Sn from the bulk **solder** for the growth of interfacial IMC layer and flattening of the **solder**/IMC layer during isothermal aging of the **solder** joint.
Subfile: A

37/3,AB/14
DIALOG(R)File 2:INSPEC

5606088 INSPEC Abstract Number: A9714-6810-008
Title: The spreading **kinetics** of Ag-28Cu/sub (L)/ on **nickel** /sub (S)/. II. Area of spread on surfaces plated with electrolytic **Ni**
Author(s): Weirauch, D.A., Jr.; Horvath, S.F.
Author Affiliation: Alcoa Center, PA, USA
Journal: Journal of Materials Research vol.12, no.4 p.953-64
Publisher: Mater. Res. Soc,
Publication Date: April 1997 Country of Publication: USA
CODEN: JMREEE ISSN: 0884-2914
SICI: 0884-2914(199704)12:4L.953:SK2N;1-3
Material Identity Number: I870-97005
U.S. Copyright Clearance Center Code: 0884-2914/97/$2.50
Language: English
Abstract: Furnace **brazing** is commonly used in the electronic industry to attach I/O pins, lid-seal rings, and heat spreaders to cofired multilayer ceramic packages. Despite the widespread industry usage of electrolytic and electroless **Ni** coatings to render base metal surfaces wettable by **braze** fillers, there is no fundamental treatment of "**brazeability**" in the published literature that can be used by the materials technologist to design coatings for a given application. In this study, dynamic hot stage microscopy is used to establish the parameters that control the spreading of **eutectic** Ag-Cu **braze** on surfaces plated with electrolytic **Ni** . The effects of plating thickness, substrate type, plating annealing, and the **braze** thermal cycle are considered. A **braze** spreading mechanism developed for polycrystalline **Ni** foil in Part I of this study is linked to **Ni**-plated surfaces through consideration of differences in microstructure. Eventual extension of this improved understanding to surfaces plated with electroless **Ni** -B and **Ni**-P deposits will result in shortened product design time and improved manufacturing, process control.
Subfile: A

37/3,AB/15
DIALOG(R)File 2:INSPEC

5578728 INSPEC Abstract Number: B9706-0170J-049
Title: Aging studies of Cu-Sn intermetallic compounds in annealed surface mount **solder** joints
Author(s): So, A.C.K.; Chan, Y.C.; Lai, J.K.L.
Author Affiliation: Dept. of Electron. Eng., City Univ. of Hong Kong, Kowloon, Hong Kong
Journal: IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging vol.20, no.2 p.161-6
Publisher: IEEE,
Publication Date: May 1997 Country of Publication: USA
CODEN: IMTBE4 ISSN: 1070-9894
SICI: 1070-9894(199705)20:2L.161:ASIC;1-V
Material Identity Number: B481-97002
U.S. Copyright Clearance Center Code: 1070-9894/97/$10.00
Language: English
Abstract: Our previous investigation (1995), revealed the formation **kinetics** and characteristics of copper-tin (Cu-Sn) intermetallic compounds (IMC) in leadless ceramic chip carrier (LCCC) surface mount **solder** joints during infrared (IR)-reflow **soldering** . The

present study focuses on the solid state growth of the interfacial Cu-Sn IMC in LCCC surface mount **solder** joints under prolonged annealing at elevated temperature. A thick Cu-Sn IMC layer at the Sn-Pb **solder**/Cu interface of a surface mount **solder** joint (which can be achieved by prolonged aging at high temperature or after long term operation of surface mount technology (SMT) electronic assemblies) makes the interface more sensitive to stress and may eventually lead to fatigue failure of all SMT **solder** joint. The microstructural morphology of the Cu-Sn IMC layer at the **solder**/Cu pad interface in all annealed LCCC surface mount **solder** joints is duplex and consists of eta -phase Cu/sub 6/Sn/sub 5/ and epsilon -phase Cu/sub 5/Sn IMC. Both Cu-Sn LMC phases thicken as the aging time increases. On the other hand, at the interface close to the component metallization, the growth of both the eta - and epsilon -phase were shown to be suppressed, with more a pronounced effect on epsilon -phase, by **Ni** originating from the metallization. The mean total layer thickness was found to increase linearly with the square root of aging time and the growth was faster for higher annealing temperature. The activation energy for the growth of interfacial Cu-Sn IMC layers and the pre-exponential factor, D/sub 0/, for diffusion were found to be 1.09 eV and 1.68*10/sup -4/ m/sup 2//s, respectively, for the 0805 LCCC surface mount **solder** joint using **eutectic** Sn-Pb **solder**. The pad size and quantity of Sn-Pb **solder** employed in LCCC surface mount **solder** joints were shown to have little effect on the solid state growth rate of interfacial Cu-Sn IMC layers.

Subfile: B

37/3,AB/16
DIALOG(R)File 2:INSPEC

5430593 INSPEC Abstract Number: B9701-0170J-045

Title: Aging studies of Cu-Sn intermetallic compounds in annealed surface mount **solder** joints

Author(s): So, A.C.K.; Chan, Y.C.

Author Affiliation: Dept. of Electron. Eng., City Polytech. of Hong Kong, Kowloon, Hong Kong

Conference Title: 1996 Proceedings. 46th Electronic Components and Technology Conference (Cat. No.96CH35931) p.1164-71

Publisher: IEEE, New York, NY, USA

Publication Date: 1996 Country of Publication: USA 1311 pp.

ISBN: 0 7803 3286 5 Material Identity Number: XX96-01869

U.S. Copyright Clearance Center Code: 0 7803 3286 5/96/$4.00

Conference Title: 1996 Proceedings 46th Electronic Components and Technology Conference

Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc

Conference Date: 28-31 May 1996 Conference Location: Orlando, FL, USA

Language: English

Abstract: This is the second in a series of investigations aimed at studying the effect of Cu-Sn intermetallic compound on the reliability of surface mount **solder** joints. Our previous investigation revealed the formation **kinetics** and characteristics of Cu-Sn intermetallic compounds in LCCC surface mount **solder** joints during IR-reflow **soldering**. The present study focuses on the solid state growth of the interfacial Cu-Sn intermetallic compound in LCCC surface mount **solder** joints under prolonged annealing at elevated temperature. A thick Cu-Sn IMC layer at the Sn-Pb **solder**/Cu interface of a surface mount

solder joint (which can be achieved by prolonged storage at high temperature or after long term operation of modern SMT electronic assemblies) makes the interface more sensitive to stress and may eventually lead to fatigue failure of all SMT **solder** joint. The microstructural morphology of the Cu-Sn IMC layer at the **solder**/Cu pad interface in all annealed LCCC surface mount **solder** joints is duplex and consists of eta -phase Cu/sub 6/Sn/sub 5/ and epsilon -phase Cu/sub 3/Sn IMC. Both Cu-Sn IMC phases thicken as the aging time increases. On the other hand, at the interface close to the component metallization, the growth of both the eta - and epsilon -phase were showed to be suppressed, with more pronounced effect on epsilon -phase, by **Ni** originating from the metallization. The mean total layer thickness was found to increase linearly with the square root of aging time and the growth was faster for higher annealing temperature. The activation energy for the growth of interfacial Cu-Sn IMC layers and the pre-exponential factor, D/sub o/, for diffusion were calculated to be 1.09 eV and 1.68*10/sup -4/ m/sup 2//s respectively for the 0805 LCCC surface mount **solder** joint using **eutectic** Sn-Pb **solder** . These values are useful in predicting the thickness of interfacial Cu-Sn IMC layers in real surface mount **solder** joints in electronic assemblies after prolonged operation and hence the reliability factor of the **solder** joint attributed to the interfacial Cu-Sn IMC layer. Finally, the pad size and quantity of Sn-Pb **solder** employed in LCCC surface mount **solder** joints were shown to have an insignificant effect on the solid state growth rate for the interfacial Cu-Sn IMC layers.

Subfile: B

37/3,AB/17

DIALOG(R)File 2:INSPEC

5430582 INSPEC Abstract Number: B9701-4130-006

Title: Self-aligned, fluxless flip-chip bonding technology for photonic devices

Author(s): Kuhmann, J.F.; Hensel, H.-J.; Pech, D.; Harde, P.; Bach, H.-G.

Author Affiliation: Heinrich-Hertz-Inst. fur Nachrichtentech. Berlin GmbH, Germany

Conference Title: 1996 Proceedings. 46th Electronic Components and Technology Conference (Cat. No.96CH35931) p.1088-92

Publisher: IEEE, New York, NY, USA

Publication Date: 1996 Country of Publication: USA 1311 pp.

ISBN: 0 7803 3286 5 Material Identity Number: XX96-01869

U.S. Copyright Clearance Center Code: 0 7803 3286 5/96/$4.00

Conference Title: 1996 Proceedings 46th Electronic Components and Technology Conference

Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc

Conference Date: 28-31 May 1996 Conference Location: Orlando, FL, USA

Language: English

Abstract: The self-aligned flip-chip (FC) bonding technique is a very attractive means for the assembly of photonic devices containing multiple optical as well as electrical waveguide interconnects. In this article we propose a fluxless FC-bonding technology which nevertheless ensures efficient **solder** oxide reduction by applying molecular hydrogen (H/sub 2/) under vacuum conditions. Bonding experiments were carried out in a newly developed FC-bonder of which some interesting details are reported. Reproducable bonding accuracies below the required tolerances for fiber to tapered waveguide coupling of <or=3 mu m have been achieved. Using

eutectic tin-lead (SnPb 60/40) **solder** and **platinum** (**Pt**) as a wettable pad metallization these bonding results have been obtained at moderate temperatures (250 degrees C) and heating durations (2 min). An investigation on the oxidation **kinetics** of molten SnPb 60/40 **solder** confirms the ability of H/sub 2/ to reduce **solder** oxides when thermodynamic boundary conditions are met. The leach resistance of the **Pt** thin-film metallization (300 nm) has been prooved by SIMS depth profiles for the required bonding temperatures and durations.
Subfile: B

37/3,AB/18
DIALOG(R)File 2:INSPEC

5388895 INSPEC Abstract Number: A9622-8265-003, B9611-0170G-008
Title: Interfacial reactions during **soldering** with lead-tin **eutectic** and lead (Pb)-free, tin-rich solders
Author(s): Kang, S.K.; Rai, R.S.; Purushothaman, S.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: Journal of Electronic Materials vol.25, no.7 p.1113-20
Publisher: TMS,
Publication Date: July 1996 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
SICI: 0361-5235(199607)25:7L.1113:IRDS;1-Q
Material Identity Number: J246-96009
Language: English
Abstract: The use of lead (Pb)-containing solders for the interconnections of microelectronic subsystem assembly and packaging has become an environmental issue. Extensive research and development activities for replacing Pb-containing solders with environmentally safe Pb-free solders are in progress in electronic industries, universities, and national laboratories. One key technical issue recognized with the Pb-free, Sn-rich solders is a need to develop a good barrier metallurgy to control the interfacial reactions, namely, dissolution of the base metal(s) and concurrent formation of intermetallics at the **soldering** interfaces. In this study, the interfacial reactions of Cu and **Ni** metallization with several Pb-free and Pb-containing solders are investigated. The dissolution **kinetics** of the base metal(s) as well as the growth **kinetics** of the intermetallics are discussed.
Subfile: A B

37/3,AB/19
DIALOG(R)File 2:INSPEC

5176703 INSPEC Abstract Number: B9603-0170G-010
Title: Interfacial reactions with lead (Pb)-free solders
Author(s): Rai, R.S.; Kang, S.K.; Purushothaman, S.
Author Affiliation: IBM Res. Div., IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference (Cat. No.95CH3582-0) p.1197-202
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 1293 pp.

ISBN: 0 7803 2736 5 Material Identity Number: XX95-01395
U.S. Copyright Clearance Center Code: 0569-5503/95/0000-1197$3.00
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference
Conference Date: 21-24 May 1995 Conference Location: Las Vegas, NV, USA
Language: English

Abstract: **Solder** interconnection technology plays a key role in various levels of microelectronics packaging, such as controlled collapse chip connection (or C4), **solder**-ball connection in ball-grid-array (BGA), or IC package assembly to a printed circuit board (PCB). **Soldering** technologies employed in these applications are quite different in terms of **solder** materials and processes. The metallurgical phenomena, however, during the **soldering** processes are very similar to each other, such as wetting of a molten **solder** to a metallic surface, dissolution of the base metal into the molten **solder**, formation of intermetallics, and **solder** joint formation by solidification. A good understanding and thereby the control of the interfacial reactions, namely, dissolution of the base metal(s) and concurrent formation of intermetallics at the **soldering** interfaces, are critical in producing sound and reliable **solder** joints. In the present paper, the interfacial reactions of Cu and **Ni** base metals with several Pb-free solders at their corresponding reflow temperatures are investigated. The interfacial reactions studied simulate the solid-liquid reaction which occurs during the initial **solder** joint formation as well as its rework process, if necessary. The Pb-free solders used in this investigation include; 58%Bi-42%Sn, 96.5%Sn-3.5%Ag, 95%Sn-5%Sb, and 100%Sn. The Sn/Pb **eutectic solder** is also included as a bench mark to compare the reaction **kinetics** with those of the Pb-free solders. The dissolution **kinetics** of Cu and **Ni** into the Pb-free solders as well as the growth **kinetics** of the intermetallic phases are measured using cross-sectional metallography of reaction couples and are compared with those obtained from the Sn/Pb **eutectic solder**.

Subfile: B

37/3,AB/20
DIALOG(R)File 2:INSPEC

4641728 INSPEC Abstract Number: B9405-0530-003
Title: The dependence of the activation energies of intermetallic formation on the composition of composite Sn/Pb solders
Author(s): Pinizzotto, R.F.; Jacobs, E.G.; Wu, Y.; Sees, J.A.; Foster, L.A.; Pouraghabagher, C.
Author Affiliation: Center for Mater. Characterization, North Texas Univ., Denton, TX, USA
p.209-16
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA x+4111 pp.
ISBN: 0 7803 0782 8
U.S. Copyright Clearance Center Code: CH3194-8/93/0000-0209$01.00
Conference Title: Proceedings of IEEE International Reliability Physics Symposium
Conference Sponsor: IEEE
Conference Date: 23-25 March 1993 Conference Location: Atlanta, GA, USA
Language: English

Abstract: The **kinetics** of the growth of Cu/Sn intermetallics at composite **solder** /Cu substrate interfaces is examined. The composite solders consist of a **eutectic** Sn/Pb matrix plus additions of Cu, Cu/sub 6/Sn/sub 5/, Cu/sub 3/Sn or **Ni** particles. Samples were annealed at 110 to 160 degrees C for up to 64 days. The activation energies measured for Cu/sub 6/Sn/sub 5/ and Cu/sub 3/Sn formation with the **eutectic solder** alone are in good agreement with previously published values. The Cu-containing particles increase the activation energy for Cu/sub 6/Sn/sub 5/ formation and reduce the activation energy for Cu/sub 3/Sn. It is proposed that the particles (1) act as Sn sinks and (2) reduce the cross-sectional area of Sn diffusion. **Ni** is a diffusion barrier which prevents Sn from diffusing into Cu. It drastically increases the activation energies for the formation of both Cu/Sn intermetallics. Only Cu/sub 6/Sn/sub 5/ with a substantial volume fraction of voids is observed for this composite **solder**. The voids form on the Cu side of the intermetallic due to differential mass transport.
Subfile: B

37/3,AB/21
DIALOG(R)File 2:INSPEC

04040310 INSPEC Abstract Number: A9202-8160B-004
Title: An improvement of the oxidation resistance of Ag-Cu **eutectic** -5 at.% Ti **brazing** alloy for metal/ceramic joints
Author(s): Xian, A.P.; Si, Z.Y.; Zhou, L.J.; Shen, J.N.; Li, T.F.
Author Affiliation: Inst. of Metal Res., Acad. Sinica, Shenyang, China
Journal: Materials Letters vol.12, no.1-2 p.84-8
Publication Date: Sept. 1991 Country of Publication: Netherlands
CODEN: MLETDJ ISSN: 0167-577X
U.S. Copyright Clearance Center Code: 0167-577X/91/$03.50
Language: English
Abstract: The oxidation **kinetics** of the Ag-Cu **eutectic**-5 at.% Ti **brazing** alloy for metal/ceramic joints was studied by the TGA technique and X-ray diffraction. The results revealed that the oxidation resistance of the alloy was very poor, but can be improved by adding 5 at.% Al to form an adherent protective CuAl/sub 2/O/sub 4/ film without sacrificing its excellent wettability, whereas small additions of Cr, **Ni** or RE were ineffective.